ABSTRACT

A method for fabricating dielectric barrier layers in integrated circuit structures such as damascene structures is provided. In one embodiment, a low-k dielectric layer formed on a substrate is provided. The low-k dielectric layer has at least one opening exposing an underlying metal layer. A first silicon carbide barrier layer is formed to conformally cover the exposed surfaces of the opening. A portion of the first silicon carbide barrier layer above the low-k dielectric layer and over the bottom of the opening is converted with an oxidation treatment into a layer of silicon oxide. The silicon oxide layer is removed above the low-k dielectric layer and from the bottom of the opening. The opening is filled with a conductive layer in electrical contact with the underlying metal layer. The conductive layer is removed above the low-k dielectric layer to a predetermined depth below the low-k dielectric layer to define a recess therebelow. A second silicon carbide barrier layer is formed to cover the recess and above the low-k dielectric layer and the first silicon carbide barrier layer so as to seal the top of the structure. A portion of the second silicon carbide barrier layer above the low-k dielectric layer is converted with an oxidation treatment into a layer of silicon oxide. The layer of silicon oxide is then removed and the metal conductive layer is fully encapsulated by the silicon carbide barrier layer.